

WHAT IS CLAIMED IS:

- 1 1. A method for chip testing, comprising the steps of:
 - 2 establishing a communications link between a chip and a computer tester;
 - 3 receiving on the chip an initial test algorithm over a communications link;
 - 4 testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance
 - 5 with the initial test algorithm;
 - 6 collecting a set of failure information in response to the testing; and
 - 7 transmitting the failure information from the chip to the computer over the
 - 8 communications link.

- 1 2. The method of claim 1, wherein:
 - 2 the receiving step includes the step of receiving a second test algorithm whose
 - 3 coverage differs from the initial test algorithm; and
 - 4 the testing step includes the step of testing the chip in accordance with the second
 - 5 test algorithm.

- 1 3. The method of claim 1, wherein the testing step includes the step of:
 - 2 testing a memory array within the chip in accordance with the algorithm.

- 1 4. The method of claim 3 further comprising the step of:
 - 2 generating a bit-map on the computer, from the failure information, of failed bit
 - 3 locations within the memory array.

- 1 5. The method of claim 3 wherein the collecting step includes the step of:
 - 2 collecting a set of failed address information in response to the testing.

- 1 6. The method of claim 5 wherein:
 - 2 the testing step includes the steps of,
 - 3 writing a set of data to an address under test in the memory array
 - 4 reading out data from the address; and
 - 5 the collecting step includes the step of adding the address under test to the set of
 - 6 failed address information, if the written set of data is not equivalent to the set of data
 - 7 read-out.

- 1 7. The method of claim 6 wherein the collecting step includes the step of:
 - 2 adding bit locations in the address under test, in which the written set of data
 - 3 differs from the set of data read-out, to the set of failed address information.

- 1 8. The method of claim 1, further including the step of:
 - 2 repairing the chip using redundancy allocation techniques based on the set of
 - 3 failure information.

- 1 9. The method of claim 1 further comprising the steps of:
 - 2 identifying a number of circuit redundancies within the chip; and
 - 3 halting testing if the failure information exceeds the number of redundancies.

1 10. A data structure for transmitting failed memory information from an on-chip built
2 in self-test circuit over a communications link to a computer, comprising:
3 a failed address field; and
4 a failed bit locations field.

1 11. The data structure of claim 3 further comprising:
2 a header field;
3 a failed address length field;
4 a failed data length field;
5 a data written field; and
6 a data read-out field.

1 12. A method for chip testing, comprising the steps of:
2 establishing a communications link between a chip and a computer tester;
3 receiving on the chip an initial test algorithm over a communications link;
4 testing a memory array within the chip, using a built-in self-test circuit (BIST) on
5 the chip, in accordance with the initial test algorithm;
6 adding an address under test and those bit locations which failed to a set of failed
7 address information, if a set of data written to the address under test is not equivalent to a
8 set of data read-out from the address under test;
9 transmitting the failed address information from the chip to the computer over the
10 communications link; and
11 generating a bit-map on the computer, from the failed address information, of the
12 failed bit locations within the memory array.

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- 1 13. A computer-readable medium embodying computer program code for commanding
- 2 a computer to perform chip testing comprising the steps of:
 - 3 establishing a communications link between a chip and a computer tester;
 - 4 receiving on the chip an initial test algorithm over a communications link;
 - 5 testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance
 - 6 with the initial test algorithm;
 - 7 collecting a set of failure information in response to the testing; and
 - 8 transmitting the failure information from the chip to the computer over the
 - 9 communications link.
- 1 14. The medium of claim 13, wherein the testing step includes the step of:
 - 2 testing a memory array within the chip in accordance with the algorithm.
- 1 15. The medium of claim 14 further comprising the step of:
 - 2 generating a bit-map on the computer, from the failure information, of failed bit
 - 3 locations within the memory array.
- 1 16. The medium of claim 14 wherein the collecting step includes the step of:
 - 2 collecting a set of failed address information in response to the testing.

1 17. The medium of claim 16 wherein:
2 the testing step includes the steps of,
3 writing a set of data to an address under test in the memory array
4 reading out data from the address; and
5 the collecting step includes the step of adding the address under test to the set of
6 failed address information, if the written set of data is not equivalent to the set of data
7 read-out.

1 18. The medium of claim 17 wherein the collecting step includes the step of:
2 adding bit locations in the address under test, in which the written set of data
3 differs from the set of data read-out, to the set of failed address information.

1 19. The medium of claim 13, further including the step of:
2 repairing the chip using redundancy allocation techniques based on the set of
3 failure information.

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1 20. A system for chip testing comprising a:
2 means for establishing a communications link between a chip and a computer
3 tester;
4 means for receiving on the chip an initial algorithm over a communications link;
5 means for testing the chip, using a built-in self-test circuit (BIST) on the chip, in
6 accordance with the initial test algorithm;
7 means for collecting a set of failure information in response to the testing; and
8 means for transmitting the failure information from the chip to the computer over
9 the communications link.

1 21. A system for chip testing, comprising:
2 a communications link;
3 a computer, operating a set of chip testing software; and
4 a chip under test coupled to the computer by the communications link, having,
5 a memory array; and
6 a Built In Self Test (BIST) module for testing the memory array in
7 response to test algorithms received from the computer and transmitting those
8 addresses within the memory array which failed testing.

1 22. The system of claim 21, wherein the chip includes:
2 redundant circuits responsive to repair programs activated on the computer in
3 response to the address failures detected during testing.